A High-Performance Si-Bipolar RF Receiver for Digital Satellite Radio

Giovanni Calì, Giuseppe Cantone, Pietro Filoramo, Guglielmo Sirna, Piero Vita, and Giuseppe Palmisano

***Abstract*— An integrated low voltage RF receiver for digital satellite radio is presented. It contains all the basic building blocks from the low noise amplifier (LNA) to the baseband buffer and two phase-locked loops (PLL's) which provide the RF and the intermediate frequency (IF) local oscillator signals. Innovative solutions for critical blocks such as the LNA, the IF buffer, the voltage controlled oscillator (VCO), etc., as well as new arrangements for bias circuits have been adopted which greatly increase circuit performance. Moreover, 2.4-V regulated power supplies with power down capability have also been included. The receiver needs a small number of external components that are principally the RF image filter and the surface acoustic wave (SAW) channel filter. It achieves a maximum gain of 120 dB and a noise figure of 5 dB. The internal regulators are set to 2.4 V and ensure correct operation with an external power supply varying from 2.7 to 5.5 V. The receiver was integrated in a high-performance 20-GHz silicon bipolar technology. Its die size is 18 mm^2 and it needs a quiescent current of 75 mA.**

***Index Terms*— Bipolar, digital satellite, IC, low voltage, RF, transceiver.**

I. Introduction

THE design of integrated RF front-ends has become a challenge in modern silicon technologies [1]. Indeed, today CMOS and bipolar processes are able to provide the high operating frequency required in an RF front-end [2]–[13]. The great interest and the widespread research effort for CMOS solutions is mainly motivated by cost reduction and the possibility for a future system on chip. However, considering today's technologies and market needs indicating a dual-chip solution, the best system partitioning in the author's opinion is associating a bipolar RF transceiver with a CMOS circuit which can easily accommodate all the baseband analog functions such as A/D and D/A converters as well as the digital signal processor. To support this suggestion, a short comparative discussion on the performance of CMOS and bipolar transistors is useful.

CMOS transistors have the inherent advantage over their bipolar counterparts of having better linearity, the potential for accurate baseband analog functions (especially if the switched capacitor approach is used), and a better capability for low-voltage and low-power digital circuits. However, bipolar transistors exhibit lower white and flicker noise and are very suitable for implementing nonlinear blocks such as balanced modulators, phase comparators, etc., which are key circuits in RF front-ends. Moreover, bipolar transistors provide a high transconductance value that, together with the low base collector capacitance, allows both high gain and frequency stability to be achieved. Further, thanks to the special dependence of the transconductance on bias current and thermal voltage, accurate open-loop gains are achieved even with large temperature variations and worst case process conditions. Finally, typical values for noise figure, signal levels, and operating frequencies in analog sections of modern RF transceivers are usually achieved with state-of-the-art CMOS processes at the expense of a higher power consumption and/or silicon area than that of bipolar processes.

For these reasons, the proposed satellite receiver was designed using a high-performance silicon bipolar technology.

The circuit is based on a dual conversion architecture with a single IF filter. It operates on a quadrature phase-shift keying (QPSK)-modulated signal whose minimum level is set to −92 dBm. To reduce common-mode noise coming from the substrate and the supply lines, a fully differential architecture was adopted and proper bias circuits were designed. The differential approach also improves stability, minimizes the risk of unwanted oscillation in high-gain blocks, and increases linearity, which is a critical performance parameter in a QPSK receiver. The circuit provides an overall gain of 120 dB and a noise figure of 5 dB. It uses a fully integrated RF oscillator which achieves a phase noise of −99 dBc/Hz at 100 kHz frequency offset.

The bit error rate with the minimum input signal level is lower than 10^{-4}.

II. System Description

A. Overall System

The overall system in which the integrated RF front-end will operate is an example of a digital satellite broadcasting radio receiver with worldwide coverage. Its main goal is to deliver audio services to those regions of the world with low population density where a terrestrial radio network is not available. Low power consumption and minimum operating voltage are very important requirements of the electronic devices in the radio because they have to be used in mobile equipment. The signal power received by the radio is suitable for a small patch antenna. The service will be provided by three geostationary orbit satellites placed in Africa, Central/South America, and Asia. Each satellite transmits three downlinks with two orthogonal polarization time division modulation

Manuscript received March 25, 1998; revised August 25, 1998.

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Publisher Item Identifier S 0018-9480(98)09228-X.

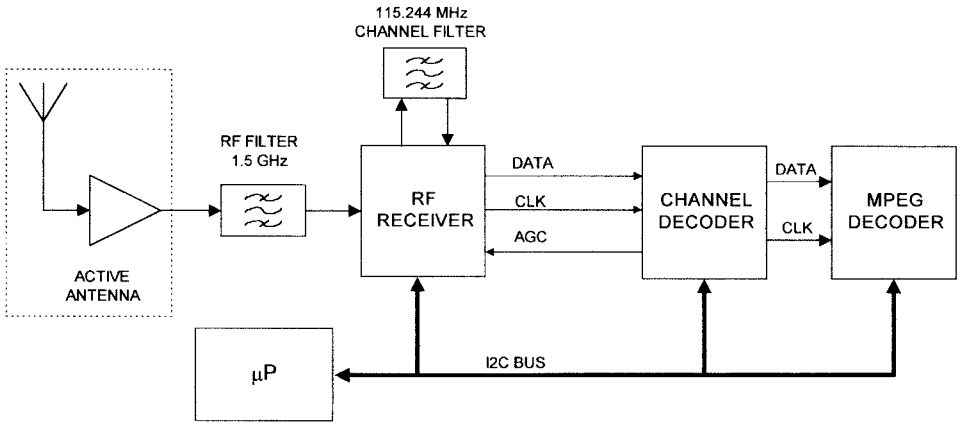


Fig. 1. System block diagram.

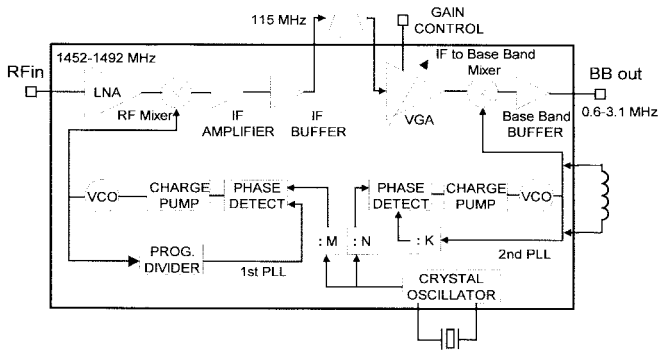


Fig. 2. Block diagram of the receiver.

(TDM) streams. The satellite carriers are in the L-Band, between 1452 and 1492 MHz.

Three dedicated integrated circuits make up the overall radio receiver as shown in Fig. 1. Their operations are controlled by a microcontroller using an I^2C bus. These chips are as follows.

- The RF receiver which converts the RF signal coming from an active antenna in a 2-MHz output. It uses minimum external components which are a ceramic bandpass RF filter for the image rejection and an IF surface acoustic wave (SAW) filter for channel selection.
- A channel decoder which includes an analog-to-digital converter, a QPSK demodulator, a signal power estimator, a TDM demultiplexer, Viterbi and Reed–Solomon decoders, deinterleaver and decryption circuits, and a broadcast channel selector.
- An MPEG decoder.

In order to guarantee a constant level at the A/D converter despite gain variations, an automatic gain control (AGC) is included between the RF receiver and the channel decoder.

B. RF Receiver

A block diagram of the proposed RF receiver is shown in Fig. 2. It includes all the basic building blocks from the RF to the baseband interface. The receiver transforms a 1.5-GHz RF signal into a 2-MHz baseband signal for the channel decoder.

The first stage is a low noise amplifier (LNA) which works in the 1.452–1.492-GHz band. Then, the RF signal is down converted by a double balanced mixer to a first 115-MHz intermediate frequency (IF). The IF signal after amplification is delivered to the channel filter by a high linear IF buffer. Due to the insertion loss of the channel filter by 23 dB, an overall gain higher than 116 dB is required with the minimum input signal condition (i.e., −92 dBm), which is 4 dB lower than the achieved one.

A gain of 50 dB occurs from the RF input to the IF buffer output. An overall high gain of the part of the receiver chain positioned before the channel filter input is necessary to make up for its high insertion loss. This prevents the excess noise produced by the blocks of the receiver positioned beyond the filter in the worst condition (i.e., minimum gain of VGA) from having considerable effect on the overall noise figure.

The RF gain is partitioned to have 20 dB in the LNA and 30 dB divided between the RF mixer and the IF buffer. This gain partitioning minimizes the risk of unwanted oscillations due to the excess of RF gain.

To compensate for the input power variations, a variable gain amplifier (VGA) was included in the receiver chain. Finally, a second conversion and a baseband buffer provide a 1-V peak-to-peak signal to the channel decoder.

The receiver includes two phase-locked loops (PLL's) for the first and second downconversion.

The PLL in the first conversion includes a real on-chip synthesizer circuit; it uses a fully integrated voltage-controlled oscillator (VCO), a programmable divider, and a digital phase comparator.

The technology isolation provided by a trench oxide approach of the high-speed bipolar process used allows for the implementation of multiple frequency synthesizers together with small signal blocks.

The reference oscillator, running at 14.72 MHz, is made up of an integrated active amplifier and an external quartz. It is also used as reference in the second PLL. The VCO in the second PLL is at 117-MHz fixed frequency and uses an external inductor.

III. Main Blocks

A. Low Noise Amplifier

A schematic of the differential LNA is shown in Fig. 3 [14]. Feedback is used to achieve an input resistance very close to

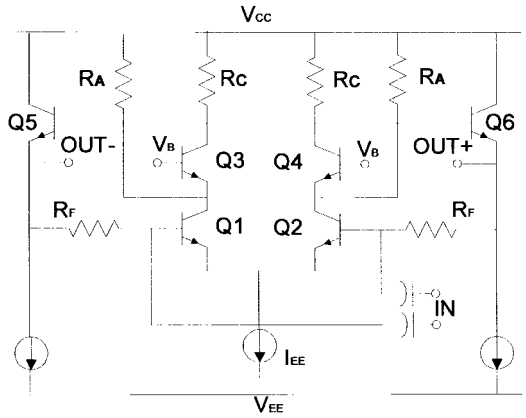


Fig. 3. Low noise amplifier.

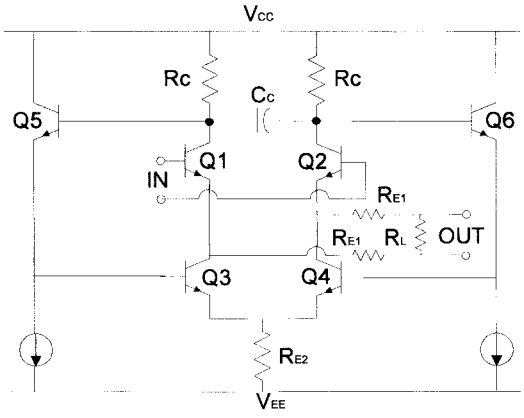


Fig. 4. IF buffer.

the source resistance. Thanks to this, the input impedance is well controlled and high return loss and low noise figure have been achieved.

The LNA is based on the cascode differential stage $Q1$–$Q4$ and is followed by the common collectors $Q5$ and $Q6$. Resistances R_F perform a shunt-shunt feedback configuration. To increase gain while avoiding output swing reduction, pump resistances R_A have been included which set the bias current in $Q1$ and $Q2$ higher than that in the load resistances R_C.

By inspection, it is easy to find that a good approximation for the differential input resistance R_i is

$$R_i \approx \frac{2R_F}{g_{m1,2}R_C} \tag{1}$$

where $g_{m1,2}$ is the transconductance of the emitter-coupled pair $Q1$–$Q2$. To provide real part impedance matching, R_i was set equal to the differential source resistance R_s.

The voltage gain A_V is given by

$$A_V = g_{m1,2}R_C. \tag{2}$$

Thanks to the PTAT bias current in $Q1$ and $Q2$, A_V is set by the ratio between poly resistances and emitter areas, and R_i is proportional to a poly resistance.

Neglecting some minor high-frequency contributions, the noise factor is approximately given by

$$F = 1 + \frac{r_{b1,2}}{R_S} + \frac{R_S}{R_F} + \frac{1}{2}\left(\frac{1}{g_{m1,2}R_S} + \frac{g_{m1,2}R_S}{\beta_F}\right). \tag{3}$$

From it, the optimum transconductance and noise factor are

$$g_{m\mathrm{opt}} = \frac{\sqrt{\beta_F}}{R_S} \tag{4}$$

$$F_{\mathrm{opt}} = 1 + \frac{r_{b1,2}}{R_S} + \frac{R_S}{R_F} + \frac{1}{\sqrt{\beta_F}}. \tag{5}$$

B. IF Buffer

The IF buffer drives the external SAW filter with a 50-Ω output impedance. Matching at the buffer output means 6 dB signal attenuation requiring an increase by 6 dB in both the gain and signal level of the IF amplifier. Therefore, giving the high gain from the LNA input to the buffer input, linearity is a very critical requirement of the IF buffer.

To increase linearity and provide an accurate output impedance matching while preserving efficiency, a class AB feedback configuration was used. The circuit is shown in Fig. 4. It is basically a differential emitter follower stage $Q1, Q2$ in which transistors $Q3$–$Q6$ and resistances R_C perform a feedback loop and where capacitor C_C provides frequency compensation. The transfer gain and the output resistance are given by

$$A_V = \frac{1}{1 + \dfrac{2}{g_{m1,2}R_E g_{m3,4}R_C}} \tag{6}$$

$$r_o = \frac{2}{g_{m1,2}g_{m3,4}R_C} \tag{7}$$

where $R_E = 2R_{E1} + R_L$ and $g_{m3,4}R_C$ is the loop gain. By setting the loop gain to unity, (6) and (7) provide the transfer gain and the output resistance without feedback, respectively. Due to the reduction of the transfer gain error by the loop gain, linearity is greatly improved. Moreover, thanks to the very low resistance at the emitter nodes of $Q1$ and $Q2$, accurate impedance matching can easily be achieved by including poly resistances R_{E1} ($R_{E1} = 25\ \Omega$).

As far as power conversion efficiency η is concerned, simple calculations give

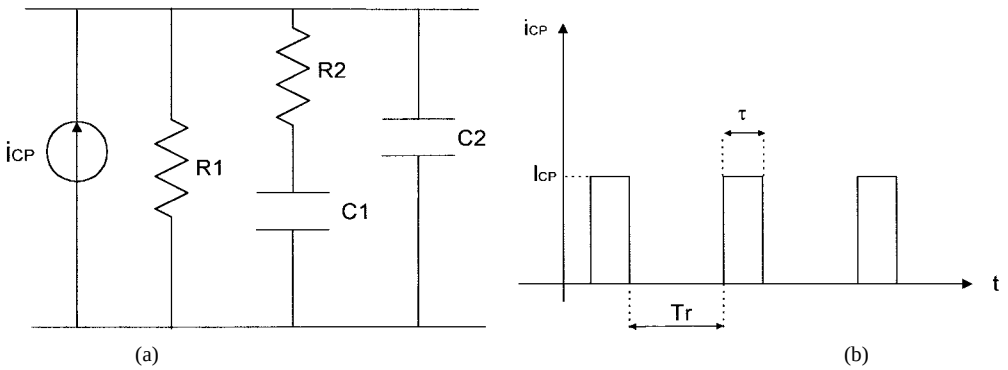
$$\eta = \frac{1}{2}\frac{V_{o\mathrm{MAX}}}{V_{CC} - V_{EE}} \tag{8}$$

where $V_{O\mathrm{MAX}}$ is the maximum output level. In our design, $V_{O\mathrm{MAX}}$ and the power supply are 0.5 and 2.4 V, respectively, and η is approximately equal to 30%.

The above formula is obtained neglecting the bias current of $Q5$ and $Q6$. In normal applications, however, these currents can be very low with respect to the overall block consumption.

C. RF PLL

In the RF PLL, the phase noise requirement is mainly achieved by the fully integrated VCO, while the bandwidth was set according to the requirement of carrier-to-spurious-rejection ratio (CSRR). In order to determine a design equation for CSRR, consider the loop filter in Fig. 5(a) and the current I_{CP} at the charge pump output in lock condition which is shown in Fig. 5(b). Time constants due to $R1$ and $C1$ ($R1 \gg$



(a) (b)

Fig. 5. (a) PLL loop filter. (b) Charge pump output in lock condition.

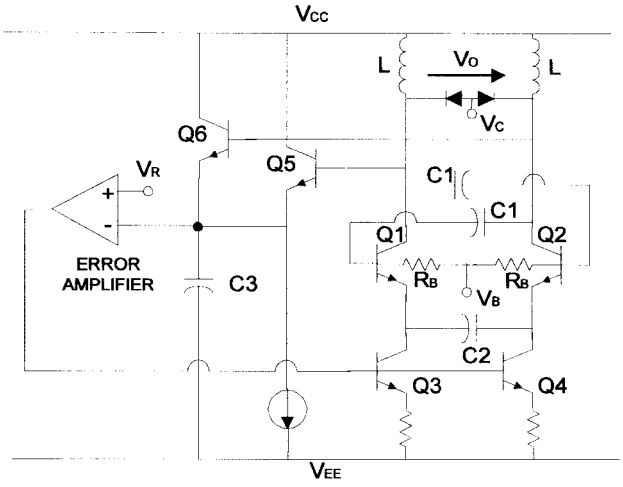


Fig. 6. VCO.

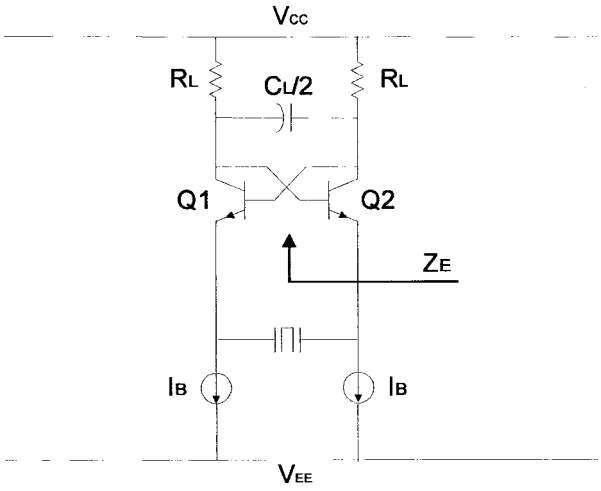


Fig. 7. Reference oscillator.

$R2$), $R2$ and $C1$ ($C1 \gg C2$), and $R2$ and $C2$ set the dominant pole, the zero, and the second pole, respectively. The period of I_{CP} is equal to the reference oscillator period T_r, and the average value (I_{AV}) of I_{CP} equals the overall leakage current I_L, which is due to both mismatch in the charge pump and saturation currents in the varactor diodes. As discussed in the Appendix, CSRR is

$$\text{CSRR} = 20\log\frac{2n^2\omega_r^2 C_2}{K_O I_n} \tag{9a}$$

where K_O is the VCO gain factor, ω_r is the reference oscillator frequency, and I_n are the harmonic amplitudes of current I_{CP} which are given by

$$I_n = I_L \frac{\sin\dfrac{n\pi I_L}{I_{CP}}}{\dfrac{n\pi I_L}{I_{CP}}}. \tag{9b}$$

Considering the value of ω_r, C_2, and K_O, which are 5.8 Mrad/s, 10 nF, and 455 Mrad/sV, respectively, and a leakage current of around 2 μA, from (9a) CSRR is greater than 57 dB.

The VCO of the RF PLL is shown in Fig. 6. It is based on integrated spiral inductors and base-collector varactors [15], [16]. The peak detector (made up of $Q5$–$Q6$ and capacitor $C3$) together with the error amplifier perform a low frequency feedback loop which sets the current in $Q3$ and $Q4$ and

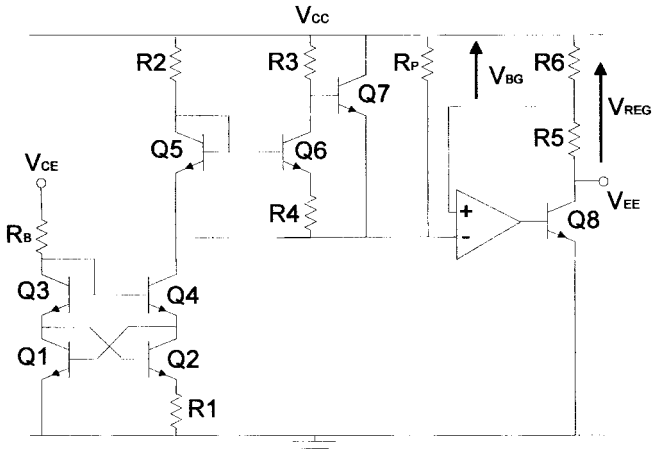


Fig. 8. Voltage regulator.

hence the oscillation amplitude to the reference voltage V_R. To increase the oscillation amplitude, ac coupling was adopted to connect the output to the input of the differential pair. Moreover, to provide high rejection to low frequency spurious signals and guarantee oscillation stability with high oscillation amplitudes, ac coupling for the emitters of $Q1$ and $Q2$ was also used.

To overcome the limitation on the tuning range due to a low percentage variation in the varactor capacitance, three

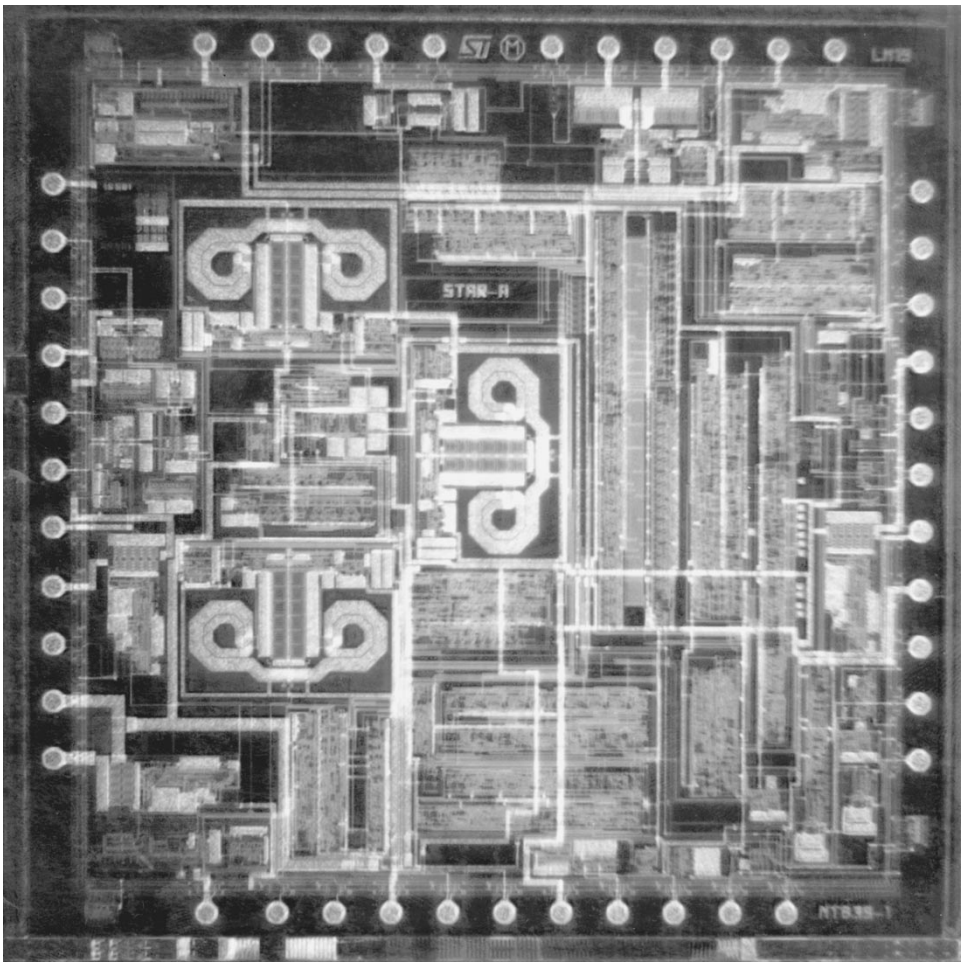


Fig. 9. Photomicrograph of the integrated receiver.

selectable oscillators with different values of varactor capacitance were implemented. Thanks to them, a wide frequency range, even in worst case conditions, is achieved.

The finite Q value of the inductors and the low frequency noise of the error amplifier (which is folded on the oscillation frequency) are the dominant contributions to phase noise. However, thanks to the high oscillation amplitude and an accurate design of the low-frequency loop, a phase noise of -99 dBc/Hz at 100 kHz was achieved.

D. Reference Oscillator

Both PLL's use the same reference oscillator shown in Fig. 7. It is a differential topology with a series resonator performed by the quartz. The main design aspects of this circuit were suppression of multiple high-frequency resonances and reduction of the parasitic inductance due to capacitor C_L and the positive feedback.

In order to avoid multiple resonances, capacitor C_L was included which reduces the loop gain to below 0 dB at undesired resonant frequencies. Indeed, the loop gain transfer function at resonance is a low-pass filter whose cutoff frequency is set by C_L and R_L.

To evaluate the parasitic inductance, let us consider the differential impedance Z_e at the emitter nodes of $Q1$ and $Q2$. Its real and imaginary parts are given by

$$R_e[Z_e] = \frac{2}{g_{m1,2}} \frac{2R_L}{1+(\omega R_L C_L)^2} \tag{10a}$$

$$I_m[Z_e] = j\omega \frac{2R_L^2 C_L}{1+(\omega R_L C_L)^2}. \tag{10b}$$

Since a small-signal model was considered, the real part of Z_e is a negative conductance. It becomes zero in steady-state condition (i.e., large-signal condition) due to the nonlinear behavior of the amplifier which reduces transconductance. Capacitor C_L in the positive-feedback amplifier is responsible for the inductive imaginary part. The parasitic inductance is in series to the quartz inductance and leads to a deviation of the resonant frequency. Moreover, due to process tolerances, the resonant frequency can only be partially compensated by a proper cut of the quartz.

The way to reduce the parasitic inductance while preserving loop gain and spurious attenuation is by reducing R_L and increasing both currents I_B and capacitor C_L. In our design, the effect of the parasitic inductance was kept lower than 30 ppm.

E. Voltage Regulator

As mentioned before, the receiver uses internal voltage regulators which provide a 2.4-V temperature-stable power supply

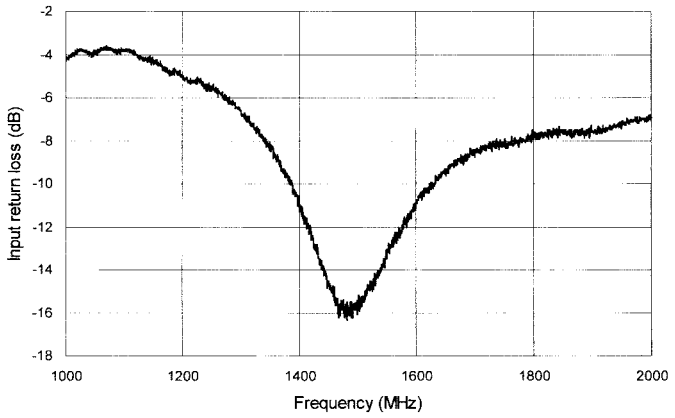


Fig. 10. Input return loss.

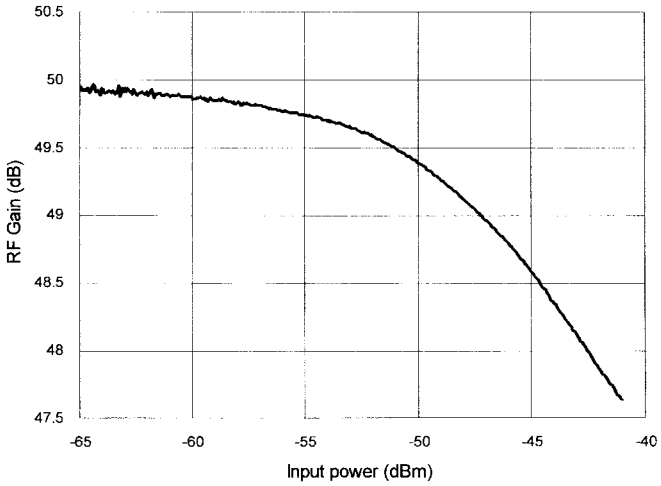


Fig. 11. Conversion gain.

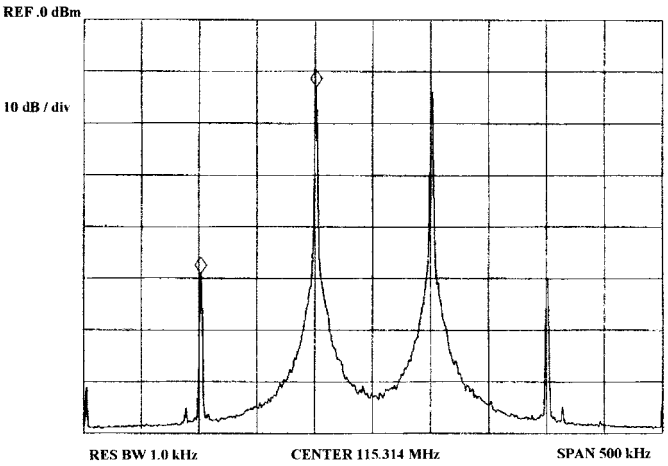


Fig. 12. Power spectrum at IF output with two input tones at −54 dBm.

and correct behavior even with variations in the external power supply. To achieve a regulated voltage even with low unregulated power supplies, voltage regulators with a common emitter output stage were used. In our case, due to the lack of good pnp transistors, positive-referred voltage regulators were designed.

A simplified schematic of the voltage regulator is shown in Fig. 8. The regulator is composed of three main blocks: a cross-coupled PTAT current generator $Q1$–$Q4$, a band-gap voltage generator $Q5$–$Q7$, and an operational amplifier which includes $Q8$ and the feedback resistances $R5$ and $R6$. The PTAT generator sets the bias current in the band-gap generator regardless of the value of V_{CE} and R_B, provided that V_{CE} is greater than $2V_{BE}$. The cross-coupled PTAT generator does not demand a start-up circuit and allows power down to be achieved easily. Indeed, the voltage regulator can be turned off simply by setting voltage V_{CE} to zero. Consequently, voltage V_{BG} and, hence, V_{REG} will both go to zero. Resistance R_P is a key element in achieving fast power down. Indeed, when current I_{PTAT} goes to zero, the inverting input of the amplifier becomes a high-impedance node and is pulled up by resistance R_P.

The regulator provides correct behavior with unregulated voltages from 2.7 to 5.5 V, needs a quiescent current lower than 0.7 mA, and is capable of delivering up to 30 mA to the load.

IV. Experimental Results

The receiver was implemented by using the high-performance bipolar technology of ST suitable for RF integrated circuit designs. It provides trench isolation and a poly-emitter npn bipolar transistor with a minimum emitter feature size of 0.4 μm and maximum transition frequency of 20 GHz. A chip photo is shown in Fig. 9. The chip was packaged in a TQFP44 using the minimum wire length for the RF inputs. Moreover, each input and output was shielded using proper supply terminals.

Experimental results were carried out on several samples with respect to the most critical parameters such as noise figure in the RF block, linearity, phase noise in the RF oscillator, etc. In the following, typical measured values are reported.

The RF input return loss is shown in Fig. 10. By using a simple two-component matching network which compensates for the parasitic elements introduced by package and bond wire, 16 dB of attenuation in the reflection signal was achieved. Under this condition, a 5-dB noise figure from the LNA to the IF buffer was measured.

Fig. 11 shows the conversion gain from the LNA to the IF buffer with an input power sweeping from −65 to −40 dBm. A gain and a $P_{1\mathrm{dB}}$ of 50 dB and a −45 dBm was achieved, respectively.

Fig. 12 shows the power spectrum at the IF output with a −54-dBm two-tone RF input signal. By applying the well-known formula ($\mathrm{IP}_3 = \mathrm{Pin} - \mathrm{IM}_3/2$), a −36-dBm IP_3 is achieved.

Two plots of the measured RF VCO power spectrum with different spans are shown in Figs. 13 and 14, and a plot of the IF VCO is shown in Fig. 15. The phase noise of the RF VCO at 100 kHz frequency offset is −69 dBc with a resolution bandwidth of 1 kHz, which means −99 dBc/Hz.

Due to the lower frequency (117 MHz) and the higher inductor Q, the IF VCO phase noise is −115 dBc/Hz at 100 kHz.

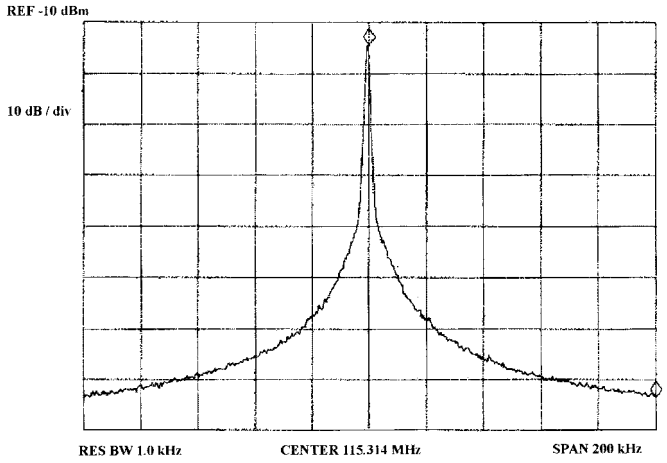


Fig. 13. RF VCO power spectrum with 200-kHz span.

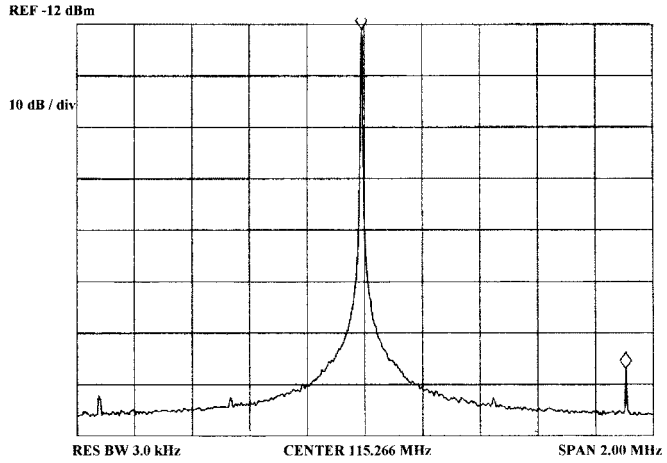


Fig. 14. RF VCO power spectrum with 2-MHz span.

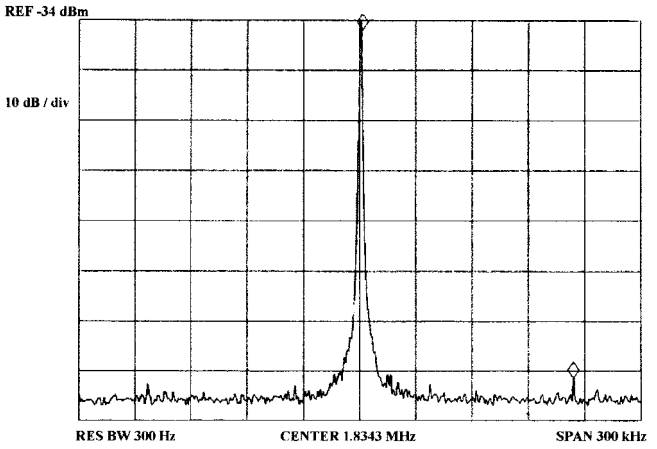


Fig. 15. Power spectrum of the IF VCO with large span.

Finally, a summary of the main electrical parameters is reported in Table I.

V. Conclusion

The proposed RF receiver is an example of a high-performance integrated front-end for the satellite radio. It includes all the basic circuits from the LNA to the baseband buffer. Two PLL's for the RF and the IF local oscillator signals are also integrated in the chip. The RF PLL is based on an integrated VCO which uses spiral inductors and standard base-collector varactors. The receiver provides a 120-dB gain and a noise figure of 5 dB allowing a bit error rate lower than 10^{-4} to be achieved. The circuit was fabricated in a silicon bipolar technology with a 20-GHz transition frequency. Several experimental results were carried out which validate its performance.

TABLE I

Overall Performance	
V_{CC}-V_{EE}	2.4 V
Maximum Gain	120 dB
Output Level	1 V_{PP}
I_{BIAS}	75 mA
Die Size	18 mm^2
LNA-Mixer	
Conversion Gain	50 dB
Noise Figure	5 dB
Input 1db c.p.	-45 dBm
Input IP3	-36 dBm
LO to RF Isolation	-60 dB
RF PLL	
Loop Bandwidth	2 kHz
Phase Noise fosc=1.35 GHz, Δf=100 kHz	-99 dBc/Hz
Spurious Rejection	64 dBc
IF PLL	
Loop Bandwidth	500 Hz
Phase Noise fosc=117 MHz, Δf=100 kHz	-115 dBc/Hz

Appendix

Carrier to Spurious Rejection Ratio (CSRR)

By expanding current i_{CP} [see Fig. 4(b)] in a Fourier series, the dc component $I_{\rm DC}$ and the harmonic amplitudes I_n are

$$I_{\rm DC} = \frac{I_{CP}\tau}{T_r} \tag{A1}$$

$$I_n = \frac{I_{CP}\tau \sin\dfrac{n\omega_r\tau}{2}}{T_r\dfrac{n\omega_r\tau}{2}}. \tag{A2}$$

Since $I_{\rm DC}$ in steady-state condition is equal to the leakage current I_L, (A1) and (A2) result in

$$I_n = I_L\frac{\sin\dfrac{n\pi I_L}{I_{CP}}}{\dfrac{n\pi I_L}{I_{CP}}}. \tag{A3}$$

Equation (A3) allows us to evaluate the amplitude of the spurious harmonics provided that leakage current is known. Of course, the first harmonic is the dominant one and mainly sets the loop-filter parameters.

Assuming, as in our case, the reference oscillator frequency ω_r higher than the second-pole frequency ω_s, the spurious harmonics at the loop-filter output are given by

$$V_n(t) \cong I_n R_1 \frac{\omega_d \omega_s}{\omega_z n \omega_r} \cos n\omega_r t \tag{A4}$$

where $R1, \omega_d$, and ω_z are the charge pump output resistance, the dominant pole frequency, and the zero frequency, respectively. By inspection of Fig. 4(a), (A4) can simply be expressed as

$$V_n(t) = \frac{I_n}{C_2 n \omega_r} \cos n\omega_r t. \tag{A5}$$

Let us now consider the VCO output voltage V_{osc} in lock condition with the spurious harmonics $V_n(t)$ applied to its input. We can write

$$V_{\text{osc}}(t) = A_o \cos \int (\omega_o + K_O V_n(t))\, dt \tag{A6}$$

where A_o, ω_o, and K_O are the VCO oscillation amplitude and frequency and gain factor, respectively. Since the phase noise deviation due to $V_n(t)$ is very small, substituting (A5) in (A6) and taking the integral we get

$$V_{\text{osc}}(t) \cong A_o \cos \omega_o t + \frac{A_o K_O I_n}{2n^2 \omega_r^2 C_2} \cdot [\cos(\omega_o - n\omega_r)t + \cos(\omega_o + n\omega_r)t]. \tag{A7}$$

The first term in (A7) is the oscillation signal, the second and third terms are the spurious at the VCO output. From (A7), CSRR in decibels is

$$\text{CSRR} = 20 \log \frac{2n^2 \omega_r^2 C_2}{K_O I_n}. \tag{A8}$$

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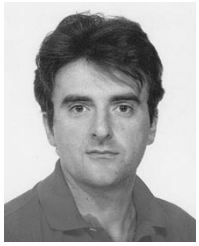

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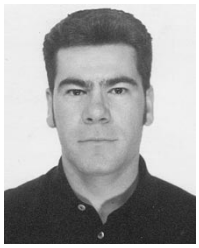

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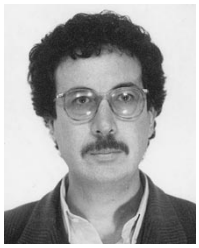

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